

XTX™ TTL Flat Panel Interface Pinout



XTX™ Specification Addendum describing valid pinout assignments for TTL flat panel interfaces

XTX™ Specification Addendum

Revision 1.0

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Revision History

Revision	Date	Author	Revision History
1.0	July 13, 06	XTX™ Consortium	Initial release

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Preface

ETX® / XTX™ Compatibility

XTX™ is an expansion and continuation of the well-established and highly successful ETX® standard. XTX™ offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications the XTX™ standard offers an array of different features on the X2 connector than those currently found on the ETX® platform.

XTX™ defines only LVDS as standard flat panel interface (fully compatible to the ETX® standard LVDS pinout). ETX® further offers an alternate pinout for TTL flat panel signals instead of the LVDS signals. As a result of different ETX® Specification releases, there are ETX® modules based on 2 different TTL display interface pinouts currently available in today's market. To allow an ETX® backward compatible XTX™ module design, use this Specification Addendum for the ETX® compatible TTL pinout description.

Carrier board designers who use this specification addendum must verify which TTL pinout assignment their XTX™ module vendor is using before implementing their carrier board TTL interface.

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Disclaimer

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Intended Audience

This XTX™ interface specification is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols may be used in this specification:



Warning

Warnings indicate conditions that, if not observed, can cause personal injury.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Note

Notes call attention to important information that should be observed.

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The XTX™ logo is freely available for members of the XTX™ consortium. The logo can only be applied to products which are fully compliant to the latest specification of the XTX™ Standard.

High resolution formats are available at the members area www.xtx-standard.org.

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1 Connector Pin Assignments

This section describes the pin assignments for the TTL flat panel interface versus the LVDS flat panel signal assignment described in the XTX Specification Rev. 1.1 or newer.

1.1 X3 Connector (LCD-TTL panel interface)

There are two signal assignment definitions that are based on two different revisions of the ETX Specification. The shaded table areas indicate the TTL signals.

1.1.1 TTL Flat Panel Interface (according to ETX Spec. 2.6 or newer)

Table 1 TTL flat panel interface signal assignments

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	B4	12	SHFCLK
13	B5	14	EN
15	GND	16	GND
17	B1	18	B3
19	B0	20	B2
21	GND	22	GND
23	G2	24	G5
25	G3	26	G4
27	GND	28	GND
29	R4	30	G1
31	R5	32	G0
33	GND	34	GND
35	R1	36	R3
37	R0	38	R2
39	VCC	40	VCC
41	FPDDC_DAT	42	VSYNC
43	FPDDC_CLK	44	BLON#
45	HSYNC	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

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1.1.2 TTL Flat Panel Interface (according to ETX Specifications older than revision 2.6)

Table 1 TTL flat panel interface signal assignments

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	B0	12	B2
13	B1	14	B3
15	GND	16	GND
17	G5	18	VSYNC
19	G4	20	HSYNC
21	GND	22	GND
23	G0	24	G3
25	G1	26	G2
27	GND	28	GND
29	R4	30	B5
31	R5	32	B4
33	GND	34	GND
35	R1	36	R3
37	R0	38	R2
39	VCC	40	VCC
41	FPDDC_DAT	42	LTGIO0
43	FPDDC_CLK	44	BLON#
45	BIOSON	46	DIGON
47	COMP	48	Y
49	SYNC	50	C
51	FLPY#	52	SHFCLK

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1.2 X3 Connector Signal Descriptions

Table 3 TTL Flat Panel Signals Descriptions

Signal	Description of TTL Flat Panel Signals	I/O	PU/PD	Comment
HSYNC	Horizontal synchronization pulse	O 3.3V		Also referred to as LP (Line Pulse)
VSYNC	Vertical synchronization pulse	O 3.3V		Also referred to as FLM (First Line Marker)
BIASON	N.A.			
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
R[0..5], B[0..5], G[0..5]	RGB Signals	O 3.3V		
SHFCLK	Panel data clock	O 3.3V		